VPX-1000S-3P-50V

1000 Watts Conduction Cooled

OpenVPX VITA 62 Compliant



KEY FEATURES:

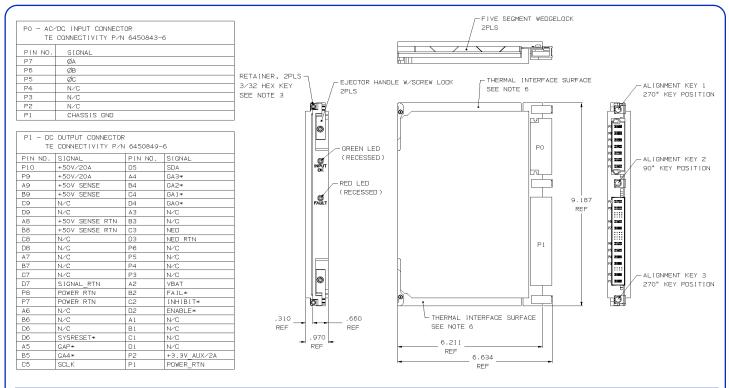
- 1000 Watts in a 6U x 5 HP (1") x 160mm Modular Design
- 3-Phase 115Vac 60Hz Input with Active Power Factor Correction (>0.98)
- Input Current THD not Exceeding 4%
- Meets MIL-STD-1399, Section 300A (Type 1) Ungrounded for the Voltage Range Specified
- VITA 62 Outputs; +50V/20A, Aux +3.3V/2A
- Custom Input/Output Configurations Available
- N+1 Redundant with Internal Oring FET's/Diodes
- VITA 62 Card Guide Style Conduction Cooled
- 1 Inch Pitch Form Factor with Wedge Lock Retainers
- Side Covers Support Two-Level Military Maintenance Requirements
- Specifically Designed for Submarine and Shipboard Applications in Compliance to MIL-STD-1399, MIL-STD-461F and MIL-STD-810G
- Ruggedized Mechanical Design
- One Year Warranty
- Greater than 150,000 Hrs MTBF







VPX-1000S-3P-50V



Nominal Input Voltage Frequency	115 Vac 3-Phase, 6A nominal. 60Hz per MIL-STD-1399 Ungrounded.	Redundant	Full power N+1 redundant with integral Oring FET's/Diodes.
Operational Input Voltage Range	+20%, -15% and transients ±25%. Input Power Factor exceeding 0.98 at full load.	Remote Sense	Compensates for up to 0.5V total distribution voltage drop on the +28V output.
Input Load Balance	Current loading for any phase does not exceed the average of the currents in all 3 phases by more than 5%.	Enable*	VITA 62 compliant. Reference SPI's VPX Signal data sheet for more details.
Inrush Current	Less than 4 msec. 40 amperes @ 115 Vac.	INHIBIT*	VITA 62 compliant. Reference SPI's VPX Signal data sheet
Fusing	(3 X 8 Ampere)/250 Vac, Very fast acting. Internal ceramic body fuses.	SYSRESET*	for more details. VITA 62 compliant. Reference SPI's VPX Signal data sheet
Hold up time	20msec minimum after loss of AC Input at full load		for more details.
Efficiency	88% typical.	FAIL*	VITA 62 compliant. Reference SPI's VPX Signal data sheet for more details.
Turn on time	1 sec max. from power up.	NED	VITA 62 compliant. Reference SPI's VPX Signal data sheet
Line and Load Regulation	±2% over AC input range and 0 to 100% load change.		for more details.
Minimum Load	No minimum load required.	VBAT	VITA 62 compliant. Reference SPI's VPX Signal data sheet for more details.
Ripple & Noise	Through 20MHz 0.5% max. or 50mv whichever is greater for both outputs, peak to peak, with coaxial	Geographical Addressing	VITA 62 compliant. Reference SPI's VPX Signal data sheet for more details.
	probe and 0.1uF/10uF capacitors at the connector.	Protocol (I ² C)	VITA 62 compliant. Reference SPI's VPX Signal data sheet
Transient Response	Output maximum excursion of ± 5% for 25% load step. Recovery less than 500 µsec.		for more details.
Overshoot	No turn-on or turn-off overshoot.	Indicators	Green LED indicating Input OK, Red LED indicating a power supply fault.
Output Isolation	Isolated from chassis ground, 100Vdc.	Cooling	Conduction cooled via wedge lock retainers.
Input/Output Isolation	1500Vdc from input to both chassis/outputs.	Operating Temperature	-40°C to 71°C (at wedge lock edge) 1000W
Reverse Voltage	Protected against reverse voltage to supply current rating.	Stability	All outputs 0.1% for 8 hrs. after 30 minute warm-up.
		Humidity	Up to 95% non-condensing.
Overvoltage	Shutdown at 130% of nominal Vout.	Storage Temperature	-55°C to 105°C.
Protection	Recycle input power to reset.	Connectors	VITA 62 compliant
Overtemperature Protection	Unit shuts down if overheated. Recycle input.	Size	6U x 5HP (1") x 160mm Weight: 3.5 lbs.
Leakage Current	1mA max at 115Vac.	EMC	Designed to meet Mil-Std-461F with SPI's external filter, Top Assembly 25930, or equivalent.
Current Limiting	All outputs protected with current limit. Automatic recovery when overload or short is removed.	Common Options	Conformal coating with Paylene & special output configurations. Consult factory for more details on a

Two or more supplies can be operated in parallel and

will share load current within 10% of each other.

Paralleling

configurations. Consult factory for more details on a

tailored solution which meets your requirements.